

Notice of Allowability

Application No.

10/003,184

Applicant(s)

REBLEWSKI, FREDERIC

Examiner

Kandasamy Thangavelu

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to June 2, 2006.
2. ☒ The allowed claim(s) is/are 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.


Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____


6/21/06

DETAILED ACTION

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Introduction

1. This communication is in response to the Applicants' communication dated June 2, 2006. Claims 14 and 30 were amended. Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 of the application are pending.

Reasons for Allowance

2. Claims 1-3, 5, 7, 8, 11, 12, 14, 19, 20, 24, 30 and 32-34 of the application are allowed over prior art of record.

3. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a hardware emulation system comprising a plurality of reconfigurable logic devices and a plurality of reconfigurable interconnect devices; the plurality of reprogrammable interconnect devices can be reprogrammably configured to provide interconnections between selected input/output terminals; the logic devices and interconnect devices are interconnected together such that multiple design signals share common input/output pins and circuit board traces; the logic circuits necessary for executing logic analyzer functions is programmed into the

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programmable resources in the logic chips of the emulation system; a plurality of emulation boards are used in the emulation system; each emulation board comprises multiple logic chips, multiple Mux chips, a co-simulation chip and a processor; the logic chips and cosim chip are attached to the event bus to route the event signals from the logic chips and cosim chip to the logic analyzer control circuitry (**Quayle et al.**, U.S. Patent 6,694,464);

(2) a built-in self-test methodology for analog-to-digital converters; the test time and test cost are reduced by moving some of the tester functions onto the chip itself; the A/D and D/A converters use on-chip processing; the number of output bits per A/D converter to be acquired by the tester and the amount of test data to be processed by the tester are reduced; for ICs with multiple A/D converters on the chip, the reduction of test bits per A/D converter allows the testing of several converters in parallel; ultimately test generation and all test data processing can be done on-chip (**de Vries et al.**, "Built-in self-test methodology for A/D converters", IEEE, 1997); and

(3) a reconfigurable multi-function computing cache architecture; in a modern microprocessor chip having cache memory, some applications may not need all cache storage; a part of the cache memory can then be reconfigured for computing as a functional unit; the reconfigurable module improves the execution time of the application; the reconfigurable cache does not result in significant delay penalty compared to a dedicated cache; the reconfigurable module works as a functional unit as well as a cache memory (**Kim et al.**, "A reconfigurable multi-function computing cache architecture", ACM 2000)

None of these references taken either alone or in combination with the prior art of record discloses a logic board designed for circuit emulation, specifically including:

(Claim 1) “wherein the on-board data processing resources are further employed to locally generate a plurality of testing stimuli and locally apply said locally generated testing stimuli to emulation circuit elements of a respective emulation IC corresponding to said partition of the IC design being emulated responsive to a testing request received through said I/O pins, and wherein at least one of said emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist said onboard data processing resources to perform said local generation and application of testing stimuli”.

None of these references taken either alone or in combination with the prior art of record discloses in an emulation apparatus, a method of operation, specifically including:

(Claim 7) “wherein the method further comprises locally generating on said logic board a plurality of testing stimuli, and applying said locally generated testing stimuli to emulation circuit elements of a respective emulation IC corresponding to said partition of the IC designs being emulated, responsive to an external testing request received by said logic board through said I/O pins of the logic board and wherein at least some of said generation of testing stimuli are performed by on-chip programmable data processing resources of said emulation ICs”.

None of these references taken either alone or in combination with the prior art of record discloses a logic board designed for circuit emulation, specifically including:

(Claim 11) “wherein at least one of said emulation ICs comprises on-chip programmable data processing resources to cooperate with and assist said on-board data processing resources to perform said local generation and application of testing stimuli”.

None of these references taken either alone or in combination with the prior art of record discloses in an emulation apparatus, a method of operation, specifically including:

(Claim 14) “wherein at least some of said generation of testing stimuli are performed by on-chip programmable data processing resources of said emulation ICs”.

None of these references taken either alone or in combination with the prior art of record discloses an emulation system, specifically including:

(Claim 19) “wherein at least one of said emulation ICs of said logic boards comprises on-chip programmable data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform said local and corresponding generation and application of testing stimuli”.

None of these references taken either alone or in combination with the prior art of record discloses in an emulation system, a method of operation, specifically including:

(Claim 24) “wherein at least some of said performances of local and corresponding generation and application of testing stimuli are assisted by on-chip programmable data processing resources of the emulation ICs of the logic boards”.

None of these references taken either alone or in combination with the prior art of record discloses in an emulation integrated circuit (IC), a method of operation, specifically including:

(Claim 30) “wherein the method further comprises locally generating testing stimuli using said on-chip programmable data processing resources; and locally applying the generated testing stimuli to an IC design being emulated, using said on-chip data processing resources”.

None of these references taken either alone or in combination with the prior art of record discloses an emulation integrated circuit (IC), specifically including:

(Claim 32) “programmable on-chip data processing resources coupled to said reconfigurable logic and interconnect resources to locally generate testing stimuli, and locally apply the generated testing stimuli to at least one of said emulated circuit elements”.

None of these references taken either alone or in combination with the prior art of record discloses in an emulation integrated circuit (IC), ... a method of operation, specifically including:

(Claim 34) “locally generating on said emulation IC testing stimuli, using programmable on-chip data processing resources; and

locally applying the testing stimuli, using said programmable on-chip data processing resources, to at least one of said emulated circuit elements”.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

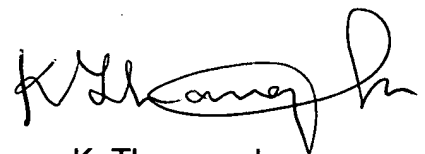
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fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

A handwritten signature in black ink, appearing to read 'K. Thangavelu', with a stylized flourish at the end.

K. Thangavelu
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June 21, 2006